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COMPRESSION AMPLIFIER

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COMPRESSION AMPLIFIER

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Technical Report Nr SELWS-E-108 October 1962

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ABSTRACT

This report discusses the design and construction of a transistorized amplitude compression amplifier and gives one application of this circuitry in the form of a Multichannel Distribution Amplifier.

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INTRODUCTION

This report discusses the design and construction of a transistorized amplitude compression amplifier and gives one application of this circuitry in the form of a Multichannel Distribution Amplifier.

The automatic gain control circuit is capable of maintaining a constant output level over a wide range of input levels, providing a high degree of stability despite component, voltage or temperature variations. By incorporating the variable impedance properties of diodes, or diode connected transistors, as one element of a variable "L" pad, and controlling this impedance by a servo-type closed loop feedback network, the system is apparently immune to both parameter variations and power supply fluctuations.

COMPRESSION AMPLIFIER

SIMPLIFIED CIRCUIT ANALYSIS

The block diagram (Figure 1) shows a simplified representation of the main section for the AC Amplifier and the AGC circuit. The AC Amplifier has a fixed gain determined by the range of input voltages to be controlled. The output of this amplifier is fed back to a peak rectifier circuit comprised of a transistor and diode. This voltage is then amplified in the DC amplifier stage which supplies the current to the variable impedance Z1. This impedance is usually comprised of one or more diodes in series, parallel, or bridge connection to give the desired dynamic impedance range when in the forward biased direction. The input signal is therefore attenuated by the variable "L" pad consisting of fixed resistor R1 and variable Z1. The operation of this pad is such that the voltage at point A is kept constant over the control range of the diodes.

A low-level input signal, at the low end of the control range of the diodes, will be amplified by the AC amplifier and arrive at the output at a predetermined level set by the gain of the amplifier. This output is then fed back through the rectifier and DC amplifier, but due to its low-level, delivers very little current to Z1. This results in a high diode impedance and no attenuation of the input signal.

If a high-level input at the maximum control level of the AGC system is applied, the fixed gain amplifier delivers a much higher output. This signal is again fed back around the loop and results in a large current in Z1, lowering its dynamic impedance. This results in considerable

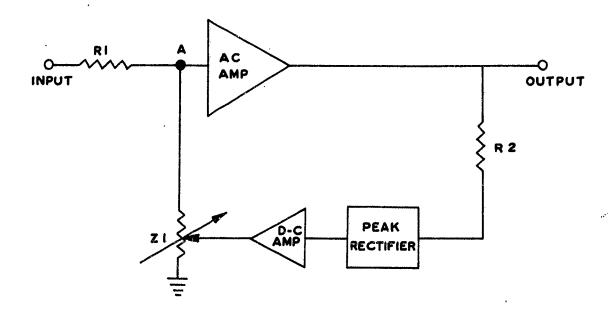


FIGURE I SIMPLIFIED BLOCK DIAGRAM

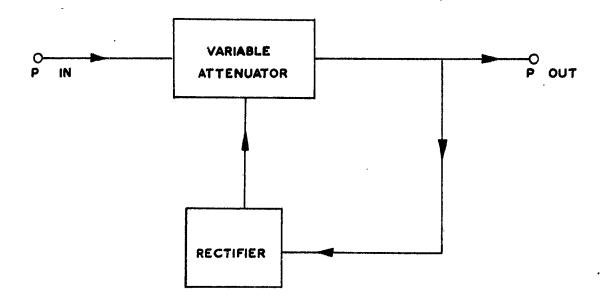


FIGURE 2 BASIC BLOCK DIAGRAM

attenuation of the input signal which, with proper adjustment of the "L" pad, now produces the same output level as the low-level signal.

The time it takes the servo loop to operate and pull down the level at point "A" is referred to as the "attack time" of the AGC circuit. For this type of circuit configuration, the "attack time" is less than 2 milliseconds.

Resistor R1 determines the output level at which the circuit operates and R2 regulates the minimum and maximum inputs at which regulation is obtained. These two values, plus the gain of the DC amplifier, are the main determining factors in obtaining the proper operating range and level for the AGC amplifier.

DETAILED CIRCUIT ANALYSIS

The variation in output level encountered for a given change in input level is known as the "stiffness ratio" of an AGC circuit and is indicated mathematically as:

$$\frac{dP_{O}}{dP_{f}} \quad \bullet \tag{1}$$

where P_{i} and P_{o} are input and output power, respectively, in db.

If the DC and AC amplifier gains are assumed to be constant, the simple block diagram of Figure 2 may be drawn, from which a mathematical analysis of the circuit can be made. From the diagram of the relationship between input power, output power and attenuation is found to be:

$$P_{o} = P_{i} - x \tag{2}$$

Also, since the diodes are current-controlled devices, the following must be true:

$$I = f_1(P_0)$$
 (3)

and the attenuation is a function of the current through the diodes:

$$x = f_2(I) \tag{4}$$

By differentiation and combination of the preceding equations, it follows that:

$$\frac{(\partial \mathbf{I}) (\partial \mathbf{X})}{(\partial \mathbf{I}) (\partial \mathbf{X})} = -\frac{\partial \mathbf{X}}{\partial \mathbf{X}} \tag{5}$$

from equation (2) supra:

$$\frac{\partial X}{\partial P_0} = -1 \text{ (a constant)} \tag{6}$$

therefore:

$$\frac{(\partial I) (\partial X)}{(\partial P_0) (\partial I)} = constant \tag{7}$$

which is the basic design equation for the circuit. The slope of the bias current versus output power curve is:

gr_o

while

is the slope of attenuation versus bias current.

Read Server

CIRCUIT DESIGN

DESIGN FACTORS

If the following step-by-step design procedure is followed, the development of a highly stable AGC circuit becomes quite simple and straightforward.

AC Amplifier

Design the AC amplifier to have a gain equal to the maximum desired output minus the lowest input level anticipated, plus about five db

as a safety margin. And if two or more stages are used, loop feedback should be added to the amplifier. The design of common-emitter amplifiers is covered sufficiently in other literature and will not be discussed here.

Feedback Loop

The design of the feedback loop starting with the rectifier circuit is as follows. The complexity of design is largely determined by the stability of the battery voltage. As would be expected, the output level of the rectifier varies considerably with fluctuations in battery voltage. If this is a problem, the supply should be regulated by the use of a Zener diode. Any convenient rectifier design can be used, as filtering is not too critical. Figure 3 shows a peak rectifier circuit employing a transistor, diodes and capacitor.

Before the design of the DC amplifier can be undertaken the type of variable impedance must be determined. The DC amplifier is strictly a linear device; that is the output current is a linear function of the input. In order to achieve rapid AGC action, it is necessary to have a nonlinear resistance as the variable element. Biodes or diode-connected transistors are therefore the obvious inexpensive solutions. Once the diode type and configurations have been decided upon, the minimum and maximum currents required can be ascertained and these then determine the specifications for the amplifier.

Diode Selection

In order for the designer to make a wise selection of the type of network to employ, pertinent diode characteristics are reviewed.

It is necessary to find a diode with a sufficiently wide dynamic impedance in the forward direction. Figure 4 is a plot of bias current versus forward impedance for a diode-connected 2N219 transistor. Silicon diodes act as linear-to-logarithmic variation in dynamic impedance for a linear input current change. The ideal relationship for the conversion is given by:

$$A = e^{CB}$$
 (8)

where A and B are variables and C is a constant. The current-voltage relationship for a diode is given by:

$$I = I_s e^{qv/k-1}$$
 (9)

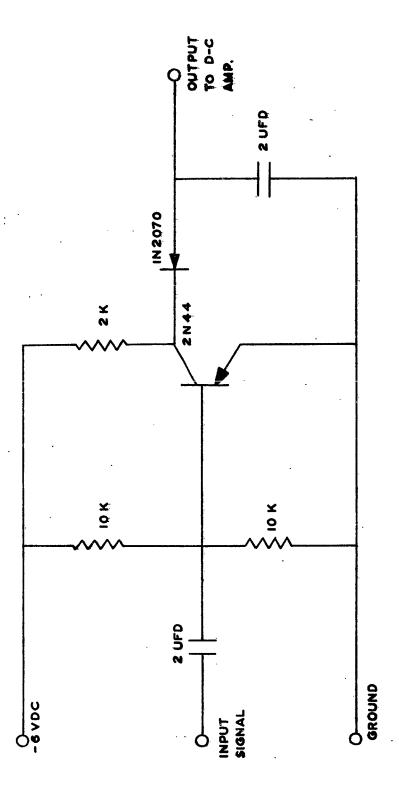


FIGURE 3 PEAK RECTIFIER

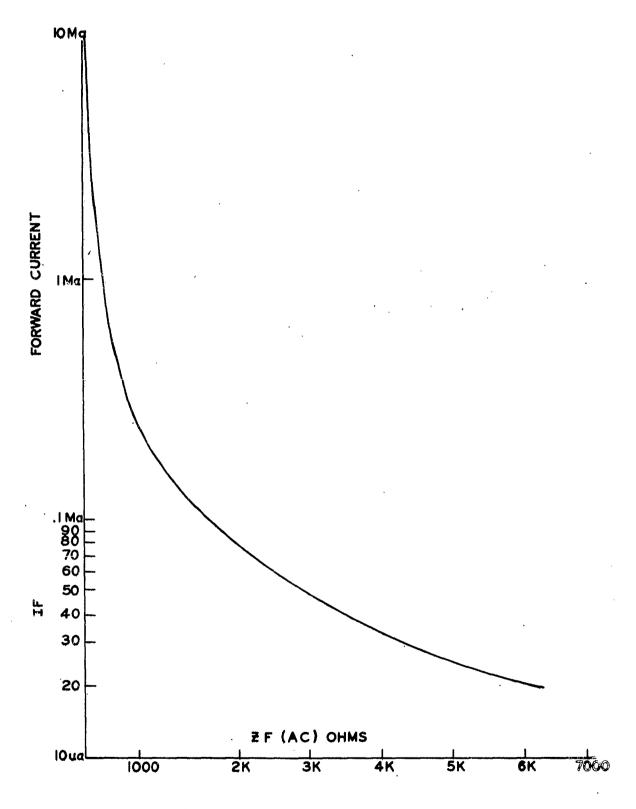


FIGURE 4 FORWARD CURRENT VS. FORWARD IMPEDANCE FOR 2N219 DIODE CONNECTED TRANSISTOR

neglecting the IR drop of the diode. At room temperature, q/kt is a constant. Also, the normal voltage across the diode is shown by:

which means that Equation 9 reduces to

$$\bar{I} = I_{se}^{CV} \tag{11}$$

where I_S (the saturation current) and C are constants. This equation is now in the form of Equation 8. Figure 5 is the V-I curve for the diode-connected 2NZ19 transistors over the range where Equation 11 is valid. The linear-to-logarithmic conversion is seen to be about 0.1 v/decade.

"L" Pad

Given the maximum input level to be controlled, the "L" pad must be so designed that it will attenuate this signal to a level equal to the minimum input plus another five db (due to the extra gain in the AC amplifier). Select some value of R1, usually in the range of 1000 to 5000 ohms. Then calculate the value of Z1 needed to give the required attenuation at the "L" pad terminal; this gives the minimum value of Z1 required. Having determined the end values of Z1 required, the necessary diode currents are readily obtained from the bias current versus forward impedance curve.

DC Amplifier

Once the range of diode currents is determined, a DC amplifier can be designed to supply these values based on the voltages available from the rectifier. Generally, a single transistor is sufficient but more can be used if needed. Difficulty is usually encountered in controlling the collector current when operation is required over a wide temperature range. The use of low I_{CO} transistors is recommended. By placing a forward-biased silicon diode in the emitter, the operating point can be more stable.

Complete Circuit

The various blocks of the circuit diagram can now be connected as shown in Figure 1. It is generally necessary to put an emitter-follower stage between the "L" pad and the AC amplifier. This isolates the two-circuits from mutual loading effects due to impedance variations. It is also advisable to make R1 and R2 variable at first so that minor adjustments can be made in operating points.

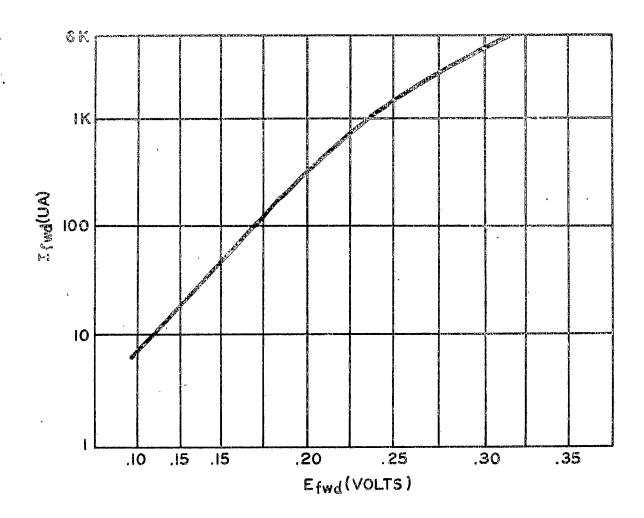


FIGURE 5 FORWARD VOLTAGE (E) VS. FORWARD CURRENT (I)

Design Example

Assume that it is required to design an AGC amplifier to give a 0 dbm output level ± 1.5 db for an input variation of -30 to ± 30 dbm. Transistor beta variation is 20 to 200 over the temperature range of 30 degrees to 130 degrees F. The battery voltage available is ± 6.0 V but can go as high as ± 8.0 V and as low as ± 4.0 V.

DESIGN PROCEDURE

To provide for output level variations due to the environmental conditions described above, the AGC circuit was designed with an allowable variation in output of 1 db for a 60 db swing in input. This means that the stiffness ratio required is:

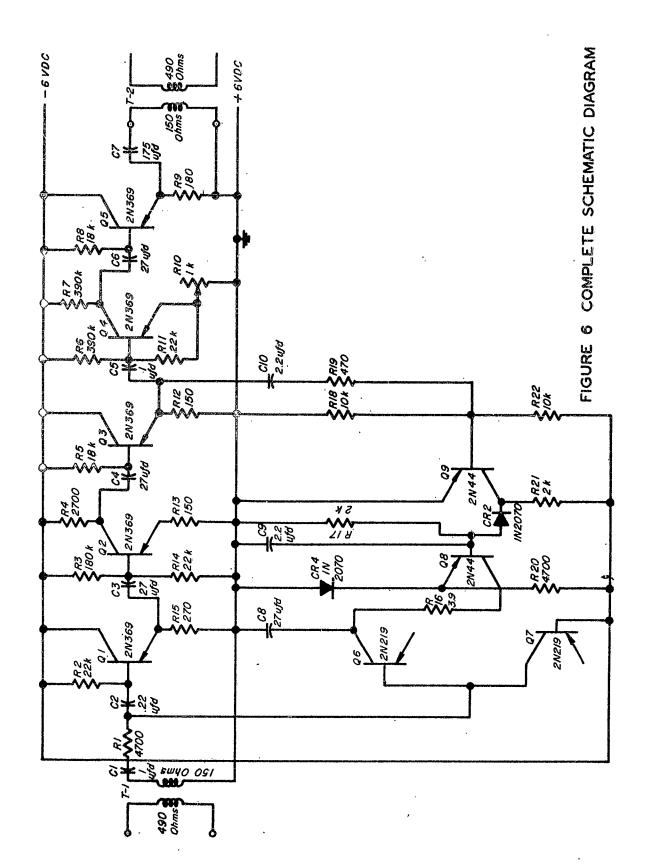
$$\frac{\mathrm{dP_o}}{\mathrm{dP_d}} = \frac{1}{60} \tag{12}$$

Step 1: First, it is necessary to design an AC amplifier of about 35 db gain. The amplifier consists of common emitter configuration containing emitter degeneration with the DC operating point stabilized by base biasing resistors. Figure 6 shows the completed amplifier. Transistors Q1 is the AC amplifier. Q9 is also an AC amplifier with variable gain so the output can be adjusted to the desired level. Q10 serves as an emitter-follower stage, providing a low impedance output suitable for driving a power amplifier or line transformer.

Step 2: The rectifier circuit is the same as previously described and shown in Figure 3. A Zener diode can be connected from collector to ground to guarantee regulation over all battery conditions.

Step 3: The next step is the design of the "L" pad. The output level at which the system must operate and the designed gain of the amplifier are known. Since the input of the amplifier must remain at a fixed value through the entire operating range, the attenuation requirements at both extremes can be calculated.

From the equivalent circuit shown in Figure 7, the required "L" pad needed to give 0 dbm output for a 0 dbm input signal can be calculated. If a value of 2700 ohms is selected for R2, V1 must be 18 mv at the input. This means that Z1 should be about 63 ohms. Referring to Figure 4 an AC impedance of 63 ohms is seen to require a very high DC current. Therefore, two diodes are used in parallel. A careful check of Figure 6 will show that diodes CR1 and CR2 are actually in parallel in an AC equivalent circuit; therefore each diode should present an impedance of



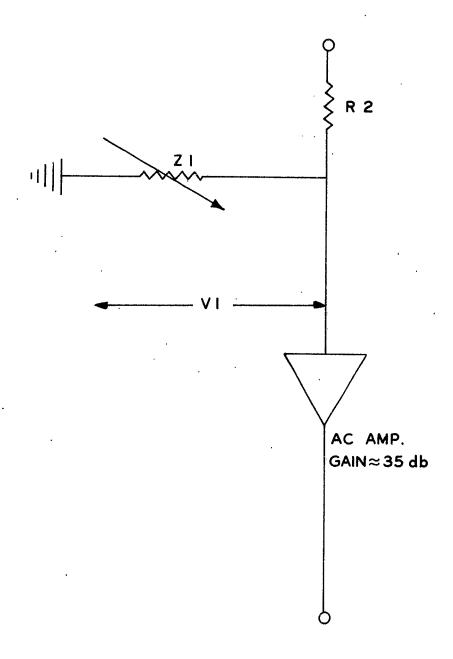


FIGURE 7 EQUIVALENT CIRCUIT

125 ohms. From Figure 4 the required bias current is approximately 2 ma.

Similarly, the value of Z1 required for an input of -30 db (24.5 mv) can be calculated. In this case, the output level can drop down to +0.5 dbm (0.825 v). This gives a value of about 1200 ohms for Z1 or an individual diode impedance of 2400 ohms and a diode bias current of 70 micro-amp. These two bias currents indicate the range of current required from the DC amplifier.

Step 4: The DC amplifier is a single stage common emitter amplifier. A special low $I_{\rm CO}$ transistor of 2 micro-amp maximum at 25 degrees C is used. A forward-biased silicon diode in the emitter further helps stabilize operation over the temperature range. A large decoupling capacitor is required in the circuit as shown in Figure $\,6$.

CONSTRUCTION

The entire unit was constructed using printed circuit techniques. Figure 8 shows the printed circuit board in actual size. A typical finished unit is illustrated in Figure 9.

TEST RESULTS

Figure 10 shows a typical frequency response of the completed unit, which is shown in Figure 6. Figure 11 typically indicates the phase shift in time versus frequency, and Figure 12 shows the total harmonic distortion with various input levels.

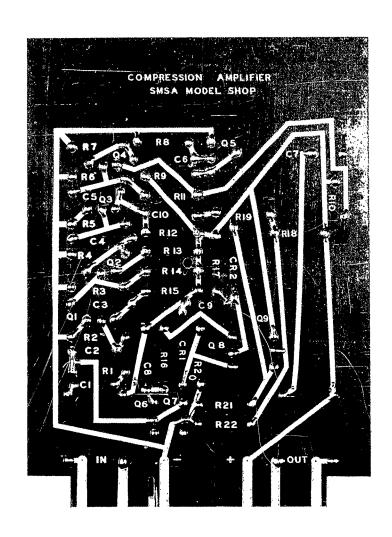


FIGURE 8 PRINTED CIRCUIT BOARD

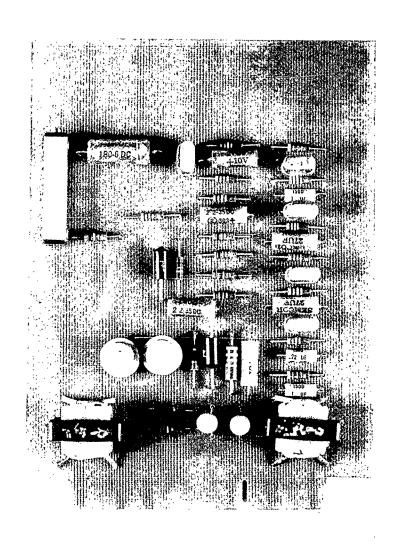


FIGURE 9 COMPLETED PRINTED CIRCUIT BOARD

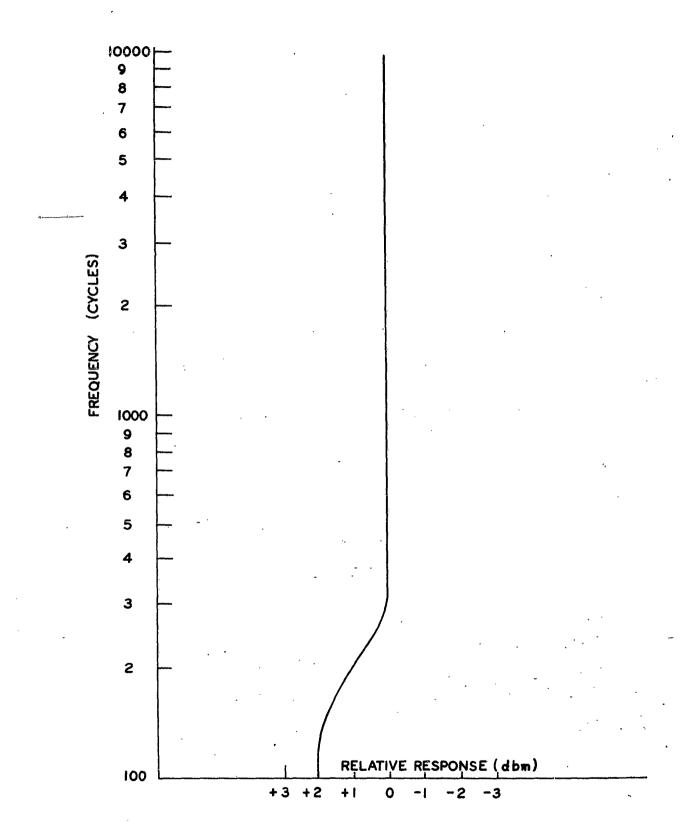
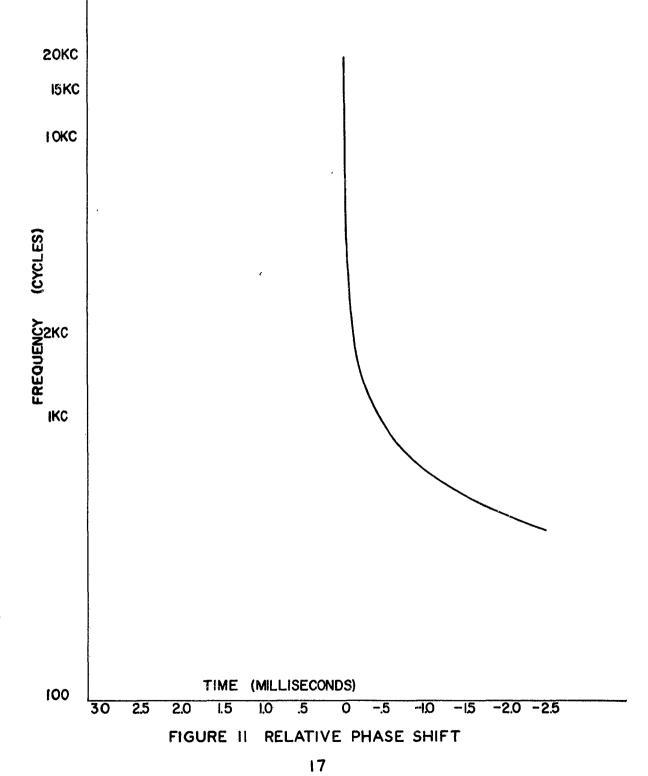
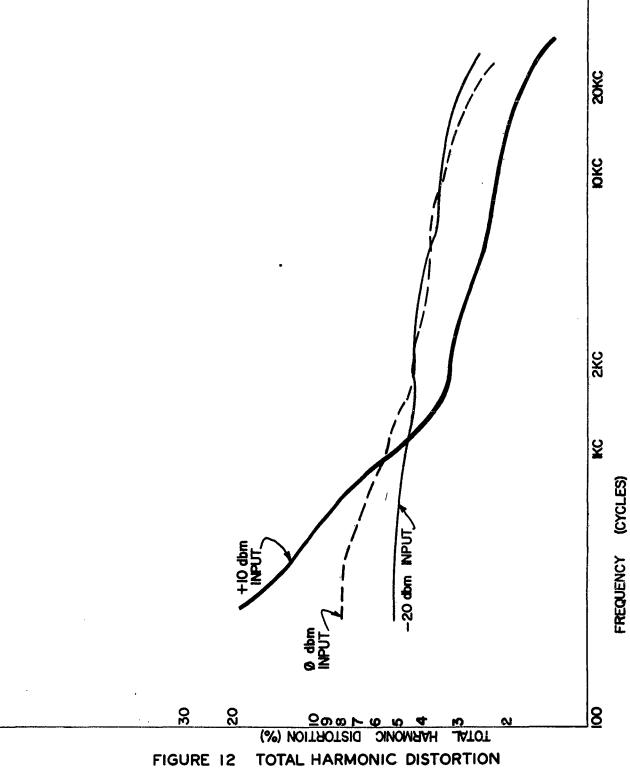


FIGURE 10 TYPICAL FREQUENCY RESPONSE





MULTICHANNEL DISTRIBUTION AMPLIFIER

PURPOSE

The transistorized multichannel distribution amplifier is a voice communications amplifier having good output level stability, with extreme variations in input audio levels. The amplifier will pass a band of audio frequencies covering the range from 300 to 3500 cycles per second. It was designed to accept audio signals, with varying input levels, for reproduction and distribution at a preset output level.

The amplifier is designed for use at remote points, to redistribute monitor signals to additional subcribers. This reduces the number of trunk circuits reflected back to the transmitting station.

TECHNICAL CHARACTERISTICS

Number of channels	Twelve
Input levels	-30 to +30 dbm
Output level	J dbm nominal, adjustable from -5 to +5 dbm
Output stability	±.5 dbm
Input impedance	600 ohms
Output impedance	600 ohms
Audio frequency response	300 to 3500 cps
Distortion	less than 5%
Power requirements	110 VAC, 60 cps
Type of mounting	standard 19 inch rack mount 5 inches high (excluding power supply)

The system is composed of twelve individual compression amplifier circuits, and one "Master" circuit. Each circuit is constructed on a plug-in type printed circuit board.

The boards may be inter-connected in any desired configuration as shown in Figure 1.

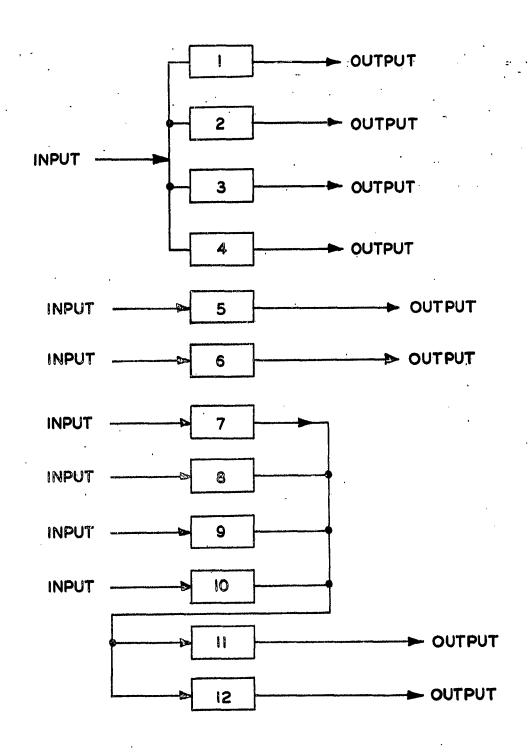


FIGURE 13 INTERCONNECTION BLOCK DIAGRAM

CIRCUIT OPERATION

The input signal is applied to the primary of transformer Tl, Figure 6 and by normal transformer action, is coupled to the secondary where it is transferred through capacitor Cl to the variable "L" pad consisting of resistor Rl and the impedance of transistors Q6 and Q7 in parallel. Only the portion of the signal that is dropped across Q6 and Q7 is applied to the base of Q1 through C2. R2 provides base bias for Q1 which is connected in an emitter follower configuration. The input signal appears across R15, and is coupled to the base of Q2 through C3. R3 and R14 form a voltage divider network which provides base bias for Q2, a common emitter amplifier. The signal applied to the base of Q2 is amplified by Q2 and coupled to Q3 by C4. R5 provides bress for Q3 which is an emitter follower. Both Q1 and Q3 provide isolation, thus preventing loading effects on Q2. The base signal of Q3 appears across emitter resistor R12, where it is continuously sampled through C10 and R19 and applied to the peak rectifier Q9. Resistors R18 and R22 form a voltage divide network which provides bias for Q9. The base signal is amplified by Q9. Crystal detector CR2 rectifies the AC signal developed across collector load resistor R21. Resistor R17 and capacitor C9 form a filter network which eliminates the ripple from the output of CR2. The input signal at the base of Q8 is a DC voltage which is proportional to the signal amplitude across R12. Transistor Q8 is a conventional DC amplifier with CR1 in the emitter circuit to aid in stability. The collector load for Q8 consists of Q6 and Q7, which are diode connected, in series. The collector current of Q8 is used to forward bias Q6 and Q7. As the forward current through Q8 and Q7, which are actually in parallel in the AC equivalent circuit, form the variable arm of the input "L" pad.

A low-level input signal will be amplified by the AC amplifier Q2, and arrive across R12 at a predetermined level set by the gain of Q2. This output is sampled and fed back through Q9 and Q8, but due to its low-level, delivers very little current to Q6 and Q7. This results in a relative high impedance across Q6 and Q7, and little or no attenuation of the input signal.

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